Theoretical Verification on the Effect of an Additional DR in Push-Push FET DROs

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***Abstract*—This letter theoretically verifies that a second Dielectric Resonator (DR) placed at the drain port of a push–push FET Dielectric Resonator Oscillator (DRO) can provide compensation for some phase difference/error between the output signals and improve the output power level. The theoretical verification starts from understanding the relationship between output power and phase in a balanced push-push oscillation scheme. The phase compensation causing power improvement is analyzed with an conceptual configuration of the circuit. The effect is confirmed by Advanced Design System (ADS) simulation for the same circuit as that in an earlier experimental report [10].**

I. Introduction

As THE MODERN communication technology progresses, higher frequency signals are required for the transmission of larger amount of information. The push-push oscillation scheme [1]–[5] is one of the many techniques used for increasing the oscillation frequency. The push-push oscillator circuit configuration basically enhances the even mode harmonics and suppresses the odd mode output, doubling the frequencies so that higher oscillating frequencies can be obtained, beyond the limitation caused by the cut-off frequency of available three terminal active devices [1]–[3]. For all types of solid-state signal sources including the push-push FET Dielectric Resonator Oscillators (DROs), even though higher frequency is necessary, maximizing output power has been the design emphasis of many applications in recent years [6]–[9].

To improve the output power of push-push FET DROs, an additional DR (Dielectric Resonator) identical to that used at the gate port was placed at the drain port [10] as shown in Fig. 1. An earlier report[10] indicated experimentally that when the second DR was tried with nine different push-push FET DROs, output power was increased by maximum 3.2 dBm at the frequency of around 19 GHz. In the report, the role of the second DR had not been theoretically investigated, and only a suggestion of the cause of the output power improvement had been made. So, it has been necessary to study the phenomenon theoretically.

In this letter, in order to theoretically verify the output power improvement of push-push FET DROs when the identical DR to that used at the gate port is added at the drain port, we first understand the relationship between the output power and the phase of the oscillators as explained in a balanced mode[11]. Secondly, the structure having a DR between two microstrip lines, as adopted in the push-push FET DRO, is simulated by High Frequency Structure Simulator (HFSS) and characterized. Thirdly, the phase compensation effect in the circuit with the additional DR is theoretically analyzed. The first, second, and third parts are described in Section II. Finally, ADS simulation confirms that the additional DR at the drain port can improve the output power as done in the previous experimental report.

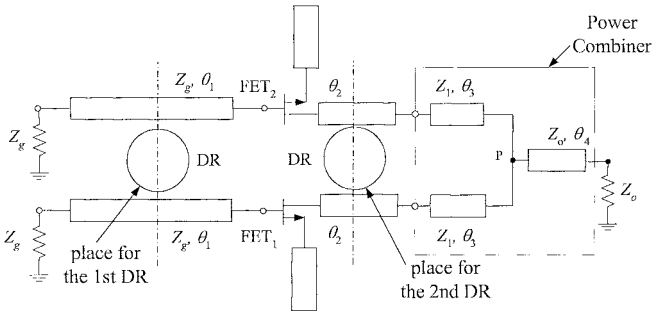

Fig. 1. Push–push FET DRO circuit configuration with an additional DR at the drain port.

II. Analysis

The relationship between the output power and the phase of push-push FET DROs begins with a qualitative understanding of the scheme having identical two single series feedback FET DROs as shown in Fig. 1. The first DR located at the gate port determines oscillation frequency and reflects the fundamental frequency components with a 180° phase difference at the gate ports so that the inputs of the active devices are controlled by two FET oscillators to be operated in a balanced mode. A power combiner is designed to cancel odd mode harmonics including the fundamental component and to enhance even mode harmonics. In this way, the second harmonic component is obtained as an output [3].

Output power levels of the fundamental and the second harmonic frequencies, $P_1(\omega)$ and $P_2(\omega)$, respectively, can be expressed in terms of phase terms [11] when bias voltages for two FETs are equal as follows:

$$P_1(\omega) \propto \left(\frac{a_o^2 A_1^2}{2} + 2a_o^2 A_2^2 V_{go} + 2a_o^2 A_1 A_2 V_{go} \right) (1 + k^2 - 2k\cos\phi) \quad (1)$$

$$P_2(\omega) \propto \frac{a_o^4 A_2^2}{8} \left(1 + k^4 + 2k^2 \cos 2\phi\right) \quad (2)$$

where a_o is the amplitude coefficient for RF input voltage of the transistor and A's are the amplitude coefficients in the relation-

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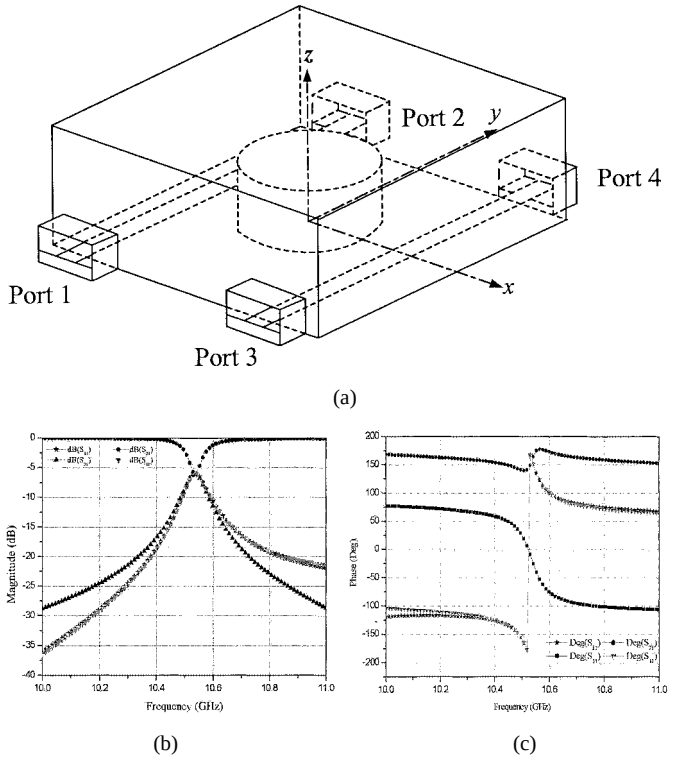

Fig. 2. (a) Simulation model, (b) magnitude response, and (c) phase response of simulated S-parameters for the structure having a DR between two microstrip lines.

ship between the output drain current and the input gate-source voltages, for each FET, respectively [11]. Equations (1) and (2) show that the output powers are dependent on the amplitude ratio, k, and the phase difference, ϕ, of the input voltages to two FETs, in a balanced operation. In the ideal balanced state $(k = 1, \phi = 0)$, the fundamental frequency components are completely cancelled and the second harmonic component enhanced by 3 dB.

To investigate the effect of the second DR placed at the drain, a structure having the identical DR used at the gate port has been simulated to obtain S-parameter response by HFSS as shown in Fig. 2(a). For the simulation, $\varepsilon_r = 2.52$ substrate with 0.54 mm thickness and 10 GHz DR (DRD051UE022: Murata) was used and a frequency range from 10 to 11 GHz was chosen. The magnitudes of S-parameters for the structure shown in Fig. 2(a), all of $\mathrm{S}_{11}, \mathrm{S}_{21}, \mathrm{S}_{31}$, and S_{41}, have about 6 dB at the resonant frequency (10.55 GHz) of the DR as shown in Fig. 2(b). This means that the coupling between microstrip lines shows band pass characteristic when transferring from port 1 to port 3, while from port 1 to port 2 it shows band reject characteristics at the resonant frequency as a directional filter. And, the phases of S_{11} and S_{31} have a 180° phase difference characteristics at the resonant frequency as shown in Fig. 2(c).

To understand the phase compensation property by the additional DR, a conceptual configuration as simplified version of Fig. 1, was considered as shown in Fig. 3, where the structure having a DR between two microstrip lines is treated as a four-port circuit and FET as a two-port circuit.

Based on Fig. 3, signal flow can be qualitatively explained as follows: input signals to the gates come out at the drains and the

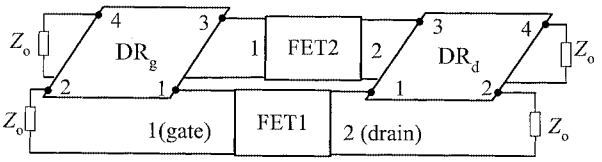

Fig. 3. Conceptual configuration of push-push FET DRO with an additional DR used in analysis for phase characteristics.

signals from the drains reflect from the additional second DR and go back to the FETs. The signals reflected back to the FETs will come out at the gates and the signals again reflect from the first DR and go back to the gates. This process is continued.

To analyze the above procedure theoretically, we assume that the two signals as expressed in (3) are applied to the gate ports. And, since the effect of the DR appears only at the fundamental frequency, ω_o, only the fundamental frequency components are only considered, whereas DC components are ignored. Thus, the voltages initially applied to the gate ports, V_{gs1} and V_{gs2}, can be written as

$$V_{\mathrm{gs1}} = a_o \cos(\omega_o t) \tag{3a}$$

$$V_{\mathrm{gs2}} = a_o k(\omega_o) \cos(\omega_o t + 180° + \phi(\omega_o)). \tag{3b}$$

If the electrical length between the first DR and the gate is θ_1 and the length between the second DR and the drain is θ_2, as shown in Fig. 1, the input signals applied to the gate ports through the above signal flow process can be written as

$$\begin{pmatrix} V'_{\mathrm{gs1}} \\ V'_{\mathrm{gs2}} \end{pmatrix} = \begin{pmatrix} S_{11}^{\mathrm{DR}_g} e^{2j\theta_1} & S_{13}^{\mathrm{DR}_g} e^{2j\theta_1} \\ S_{31}^{\mathrm{DR}_g} e^{2j\theta_1} & S_{33}^{\mathrm{DR}_g} e^{2j\theta_1} \end{pmatrix} \begin{pmatrix} S_{12}^{\mathrm{FET}} & 0 \\ 0 & S_{12}^{\mathrm{FET}} \end{pmatrix} \times \begin{pmatrix} S_{11}^{\mathrm{DR}_d} e^{2j\theta_2} & S_{13}^{\mathrm{DR}_d} e^{2j\theta_2} \\ S_{31}^{\mathrm{DR}_d} e^{2j\theta_2} & S_{33}^{\mathrm{DR}_d} e^{2j\theta_2} \end{pmatrix} \begin{pmatrix} S_{21}^{\mathrm{FET}} & 0 \\ 0 & S_{21}^{\mathrm{FET}} \end{pmatrix} \times \begin{pmatrix} V_{\mathrm{gs1}} \\ V_{\mathrm{gs2}} \end{pmatrix} \tag{4}$$

where each (2×2) matrix element contains S-parameters at resonant frequency for the two DRs and the two FETs, respectively. Since S-parameters for the two DRs are identical, (4) can be rewritten as

$$\begin{pmatrix} V'_{\mathrm{gs1}} \\ V'_{\mathrm{gs2}} \end{pmatrix} = \begin{pmatrix} S_{11}^{\mathrm{DR}} e^{2j\theta_1} & S_{13}^{DR} e^{2j\theta_1} \\ S_{31}^{\mathrm{DR}} e^{2j\theta_1} & S_{33}^{DR} e^{2j\theta_1} \end{pmatrix} \begin{pmatrix} S_{12}^{\mathrm{FET}} & 0 \\ 0 & S_{12}^{\mathrm{FET}} \end{pmatrix} \times \begin{pmatrix} S_{11}^{\mathrm{DR}} e^{2j\theta_2} & S_{13}^{\mathrm{DR}} e^{2j\theta_2} \\ S_{31}^{\mathrm{DR}} e^{2j\theta_2} & S_{33}^{\mathrm{DR}} e^{2j\theta_2} \end{pmatrix} \begin{pmatrix} S_{21}^{\mathrm{FET}} & 0 \\ 0 & S_{21}^{\mathrm{FET}} \end{pmatrix} \begin{pmatrix} V_{\mathrm{gs1}} \\ V_{\mathrm{gs2}} \end{pmatrix}. \tag{5}$$

From the HFSS analysis of the DR between two microstrip lines as we mentioned before, the following relationship can be obtained:

$$|S_{11}| = |S_{31}|, \quad \angle S_{11} = \angle S_{31} + 180° \qquad S_{11}^{\mathrm{DR}} = S_{33}^{\mathrm{DR}} = -S_{31}^{\mathrm{DR}} = -S_{13}^{\mathrm{DR}}. \tag{6}$$

Thus, (5) using (6) can be rewritten as

$$\begin{pmatrix} V'_{\mathrm{gs1}} \\ V'_{\mathrm{gs2}} \end{pmatrix} = S_{21}^{\mathrm{FET}} S_{12}^{\mathrm{FET}} \left(S_{11}^{\mathrm{DR}}\right)^2 e^{2j(\theta_1+\theta_2)} \times \begin{pmatrix} 1 & -1 \\ -1 & 1 \end{pmatrix} \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \begin{pmatrix} 1 & -1 \\ -1 & 1 \end{pmatrix} \begin{pmatrix} V_{\mathrm{gs1}} \\ V_{\mathrm{gs2}} \end{pmatrix}. \tag{7}$$

So, the signals returning to the gate ports, V'_{gs1} and V'_{gs2} can be expressed as

$$\begin{pmatrix} V'_{gs1} \\ V'_{gs2} \end{pmatrix} = 2S_{21}^{FET}S_{12}^{FET}\left(S_{11}^{DR}\right)^2 e^{2j(\theta_1+\theta_2)} \times \begin{pmatrix} 1 & -1 \\ -1 & 1 \end{pmatrix} \begin{pmatrix} V_{gs1} \\ V_{gs2} \end{pmatrix}. \quad (8)$$

By substituting (3) into (8) and rearranging, we obtain

$$\begin{aligned} V'_{gs1} &= 2a_o S_{21}^{FET}S_{12}^{FET}\left(S_{11}^{DR}\right)^2 e^{2j(\theta_1+\theta_2)} \\ &\quad \times \left[\cos(\omega_o t) + k\cos(\omega_o t + \phi)\right] \\ V'_{gs2} &= -2a_o S_{21}^{FET}S_{12}^{FET}\left(S_{11}^{DR}\right)^2 e^{2j(\theta_1+\theta_2)} \\ &\quad \times \left[\cos(\omega_o t) + k\cos(\omega_o t + \phi)\right]. \end{aligned} \quad (9)$$

Equation (9) implies that the electrical length θ_2 can be adjusted to remove the complex term $S_{12}^{FET}S_{21}^{FET}$. It also illustrates that even though the two input signals have different magnitudes and phases, the two signals will have a 180° phase difference and identical magnitudes introduced by the second DR.

Equations (3) and (4) demonstrate that the output power of a push-push FET DRO, which is the second harmonic component, will be maximized when differences in the magnitude and the phase of the gate input voltages are not present. Therefore, by placing the second DR, the magnitude and the phase differences will be compensated and a more efficient push-push oscillator may be designed.

III. Simulation Result

The above theoretical verification for the purely experimental report[10] has been confirmed additionally with ADS simulation. The simulation has been carried out with the identical circuit including the DR (DRD051UE022) and the FET (ATF-13 786) used in the experimental report. So, a push-push FET DRO generating 19.24 GHz has been designed with an intentional phase difference of input voltages at the gate by introducing slightly different electrical lengths of 0.5 mm difference between two input lines of a T-junction power combiner. Then the circuit having the second DR has been compared with the conventional circuit having single DR in terms of the phase difference between the gate input voltages and the output power levels.

Table I shows the comparison in terms of output power and phase difference between push-push FET DRO with the additional DR and that without the DR. The comparison demonstrates that the output power level has been improved with the additional DR by 2.8 dB. The phase difference has been reduced by 1.58° from 178.3 to 179.9 when there was 0.5 mm difference between the input lines of the T-junction combiner.

TABLE I
Comparison in Terms of Output Power and Phase Difference Between Push-Push FET DRO With Additional DR and Without DR

	Intentional Difference	Output Power [dBm] (@ $2f_o$)	Phase Difference [Deg]
Push-Push DRO without Additional DR	0.5 mm length difference between two input lines of T-junction	-3.008	178.309
Push-Push DRO with Additional DR	0.5 mm length difference between two input lines of T-junction	-0.199	179.888

IV. Conclusion

This letter has theoretically verified that the second DR placed at the drain port of push-push FET DRO can provide a compensation effect of both the phase and the magnitude differences/errors between the output signals from two single FET DROs constructing the push-push configuration. Thus, without changing the conventional circuit topology, the output power level of push-push FET DROs can be efficiently maximized by simply placing an additional DR at the output. If some phase and magnitude differences/errors are introduced in a design or manufacturing process, it may be beneficial to have the second DR fix the erroneous design or manufacturing process after completing the circuit production.

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